A 5.8-GHz 1-V Low-Noise Amplifier in SiGe Bipolar Technology

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ABSTRACT--A 5.8-GHz monolithic low-noise amplifier (LNA) with a minimum noise figure of 1.65 dB and an associated gain of 15 dB is implemented in a standard SiGe bipolar technology. It dissipates 13 mW from a 1-V supply (with only 9 mW in the gain stages). The measured transducer gain is 13 dB with a noise figure of 2.1 dB at 5.8 GHz. This is believed to be the lowest noise figure reported for a 5.8-GHz LNA in any production-level technology. The transducer gain is above 10 dB from 3.8 to 8 GHz. At 5.8 GHz, the input return loss and reverse isolation are 6 and 28 dB, respectively.

I. Introduction

Portable wireless data applications are extremely price sensitive and impose severe demands on low power dissipation to extend the battery life at the expense of gain and noise figure of the receiver stages. Recently emerging wireless data bands at 5 GHz and above present even more challenges for the receiver design. GaAs MESFET's and HBT's are usually considered for such C-band applications. However, state-of-the-art silicon-based technologies offer lower cost alternatives with a capability of higher levels of integration. SiGe, in particular, is a powerful high-bandwidth silicon HBT technology which can face many challenges of low-cost, low-power and low-noise receiver design [1]. A recently published single-stage 2.4-GHz SiGe low-noise amplifier (LNA) with external biasing and matching networks achieved a minimum noise figure of 0.95 dB and a 50-Ω matched noise figure of 1.75 dB [2].

In this paper, we present a low-power monolithic 5.8-GHz SiGe LNA which draws a total current of 13 mA including a reference branch bias current of 4 mA. The supply voltage used is 1 V. The 3-dB bandwidth of the amplifier extends beyond the C-band with a peak transducer gain of 13 dB. The minimum and 50-Ω noise figures at 5.8 GHz are 1.65 and 2.1 dB, respectively. The associated gain at minimum noise figure is 15 dB. Compared to the recently published 5 to 6 GHz GaAs MESFET and HBT LNA's, [3]-[4], these are believed to be the best noise figure and Gain/(P_{DC}xNoise Figure) values in any production-level technology.

II. SiGe HBT Technology

In this work, the baseline 200-mm UHV/CVD Si/SiGe HBT technology has been used without any modification. The features of the technology include transistor f_T values in excess of 45 GHz, f_{MAX} of 60 GHz, poly-silicon and diffused resistors, high-density MOS and MIM capacitors, varactor diodes and inductors [5]-[6]. The test chips are fabricated with three levels of Al metallization and conventional inter-level dielectric layers. The substrate resistivity is 10-20 Ω-cm.

III. Low-Noise Amplifier Design

A simplified schematic of the LNA is shown in Fig. 1. It is based on two common-emitter stages with inductive emitter degeneration. The output of each stage is loaded with a high-pass L-C section to increase the gain in the C-band. The AC coupling between the stages and the DC block at the output also use the same on-chip high-Q MIM capacitors of the high-pass sections. A simple on-chip biasing network provides equal base currents to each stage which can be controlled externally. In this test circuit, the bias current in the reference branch is roughly equal to the collector current of each stage, thus accounting for 1/3 of the total current consumption. It is relatively straightforward to reduce this reference current with a new design if further reduction in power consumption is required. Since only one V_{BE} drop (about 0.85 V) between the supply and ground is needed, the circuit can operate with very low supply voltages. A 28-pF MIM capacitor is used for on-chip supply decoupling and a 7-pF MIM capacitor filters the high-frequency noise of the bias reference circuit. All resistors are poly-silicon. The base currents are fed through R3 and R4 which have values around 4 kΩ.

Both gain stages and the bias network use 6x0.5x10 μm^2 effective emitter area devices (2 of 3x0.5x10 μm^2 devices shunted together) to achieve a base resistance on the order of 10 Ω or less. Each gain stage is nominally biased at 4.5 mA which is about 11%

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of the peak f_T current for this device geometry. This shows the importance of having a high-bandwidth technology to maintain low power dissipation at these frequencies. All spiral inductors are implemented by using the 2-μm thick top wiring level of this 3-level metal (Al) technology without any process modification. The total dielectric thickness under the top metal level is about 5 μm which provides very high (above 20 GHz) self-resonance frequencies for the inductors.

Simulated noise figure numbers from Libra are below 2.6 dB and 1-dB compression point and IIP3 are about -21 and -11 dBm with a transducer gain of more than 10 dB.

IV. Measured Results

The inductor values are measured on the wafer using on-chip calibration techniques and microwave probes. All the inductors have a Q of about 8 at 5.8 GHz.

The noise and scattering parameters are measured on the wafer from 2 to 10 GHz using an automated NP5 measurement system from ATN Microwave Inc. The measurements are done at two bias currents (4.5 and 2.8 mA per stage) and at two supply voltages (1 and 1.5 V). The gain and noise figure for V_{CC}=1 V and I_C=4.5 mA are shown in Fig. 2. The difference between 50-Ω and minimum noise figure is only 0.35 dB at 5.8 GHz indicating close to optimum noise match due to the large device size and six fingers used. The input and output return losses at 5.8 GHz are 6 and 4 dB, respectively. The gain can be increased further by optimizing the output match. The isolation is 28 dB. The gain and noise figure for V_{CC}=1 V and I_C=2.8 mA is shown in Fig. 3. Minimum and 50-Ω noise figure numbers degrade only by 0.05 and 0.2 dB, respectively. Both the associated gain and transducer gain are reduced by 1.6 dB, however, the power consumption of the two gain stages combined is now reduced to 5.7 mW from 9 mW.

The bias current and supply dependence of measured gain and 50-Ω noise figure values are shown in Figs. 4 and 5, respectively. The maximum to minimum gain difference is about 2 dB and the change in noise figure is about 0.2 dB at 5.8 GHz over V_{CC} =1-1.5 V and I_C=2.8-4.5 mA per stage. The variation of gain and noise figure with supply voltage is negligible.

Table 1 shows the comparison of the measured values at V_{CC}=1 V and I_C=4.5 mA to the published GaAs MESFET and HBT LNA results at 5.8 GHz. The figure of merit is defined as the ratio of transducer gain to the product of $NF_{50\Omega}$ and DC power consumption, P_{DC}. The figure of merit for the SiGe test circuit can be further improved (as indicated by the numbers in parenthesis) if the reference branch current is made negligible. Note that the potential improvement in the SiGe-LNA gain with a better output match is not taken into account in this comparison.

Table 1: Figures of merit for state-of-the-art C-band LNA's

Technology	$NF_{50\Omega}$ (dB)	S21 (dB)	P_{DC} (mW)	Fig. of Merit (mW^{-1})
SiGe HBT	2.1	13	13 (9)	0.48 (.69)
MESFET [3]	3.6	15	10	0.42
GaAs HBT [4]	2.9	16	72	0.08

The linearity measurements are done with V_{CC}=1 V and I_C=4.5 mA per stage. The measured 1-dB compression point at 5.75 GHz is -21 dBm. IIP3 measurements are performed by inserting two tones at 5.73 and 5.75 GHz. The measured IIP3 is -10.5 dBm.

The test chip micrograph is shown in Fig. 6. A first level metal ring surrounds the chip and provides a solid ground with seven large substrate contacts. This also isolates the RF pads on the top-level metal from the losses in the substrate which is crucial for noise reduction in silicon MMIC's. The input and output RF pads use GSG configuration and are located at the opposite corners of the layout to improve the isolation. The total chip area is 700x800 μm^2 including the pads and the supply decoupling capacitor.

V. Conclusions

A low-power monolithic 5.8-GHz SiGe low-noise amplifier which dissipates 13 mW (9 mW in the LNA core) with a 1-V supply is presented. The minimum and 50-Ω noise figures at 5.8 GHz are 1.65 and 2.1 dB, respectively. The associated gain at minimum noise figure is 15 dB. Compared to the 5 to 6 GHz GaAs MESFET and HBT LNA's reported recently, [3]-[4], these are believed to be the best noise figure and Gain/(P_{DC}xNoise Figure) values in any production-level technology.

VI. Acknowledgments

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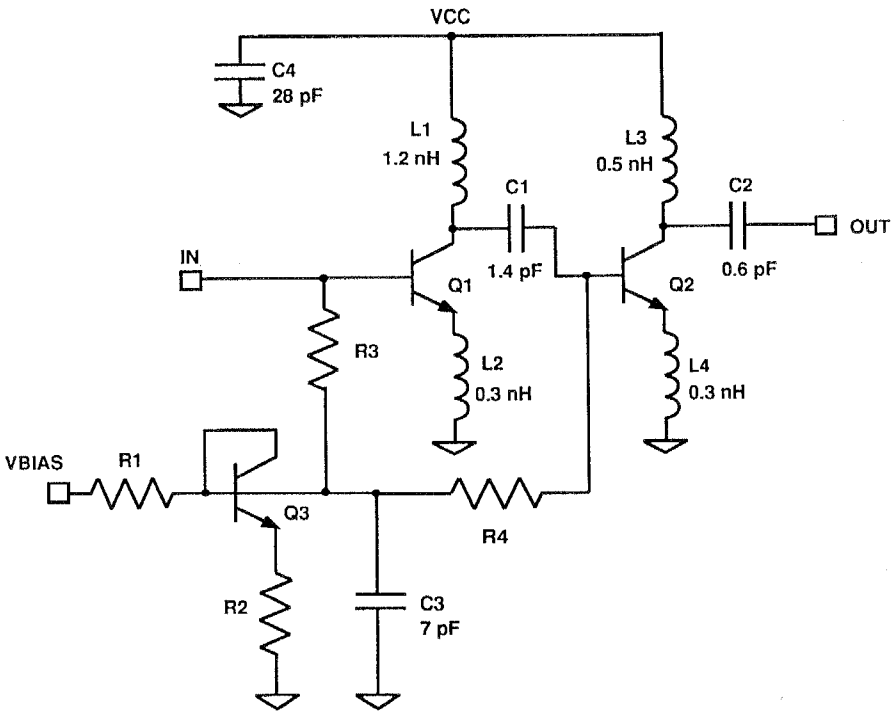

Fig. 1. Simplified schematic of the LNA.

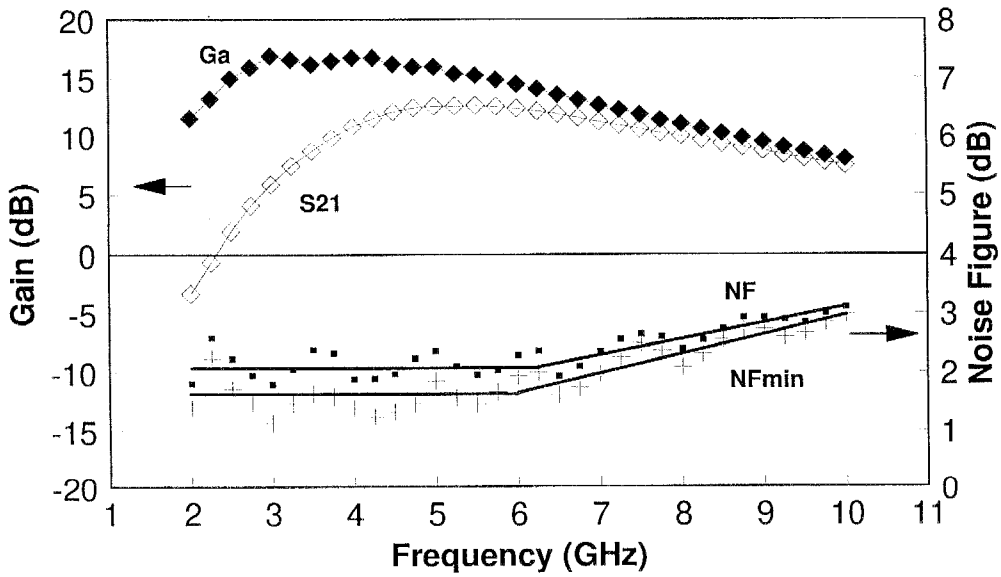

Fig. 2. Gain and NF for Vcc=1V and Ic=4.5mA/stage.

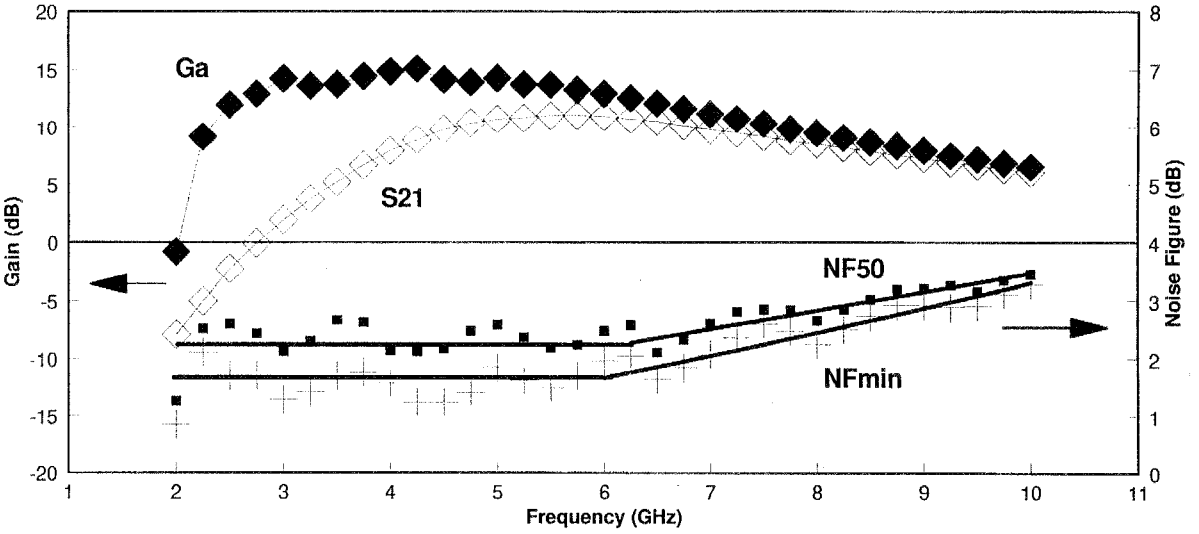

Fig. 3. Gain and NF for Vcc=1V and Ic=2.8mA/stage.

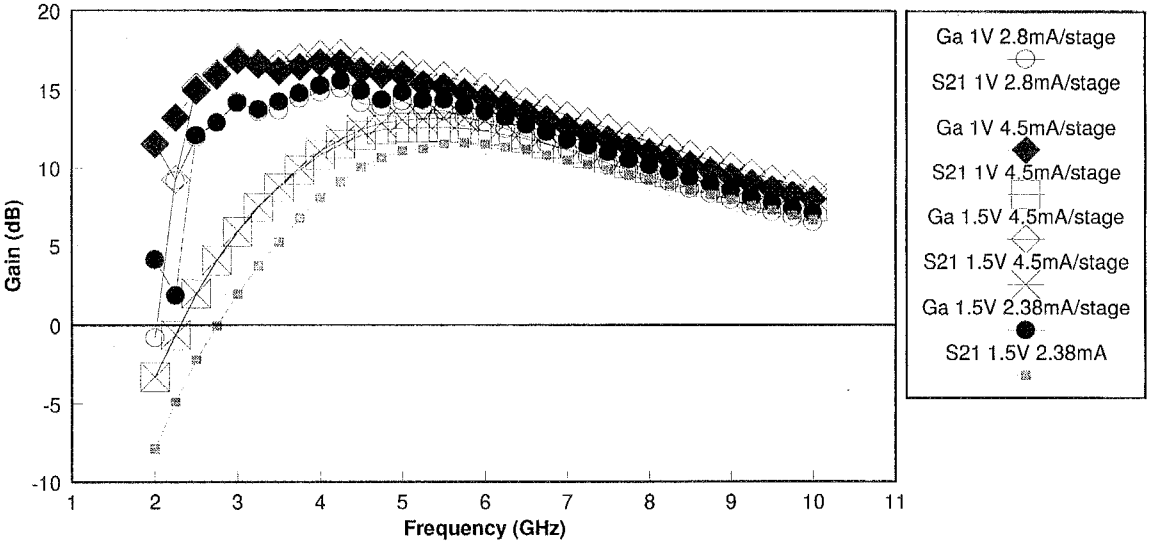

Fig. 4. Gain variation with supply voltage and bias current.

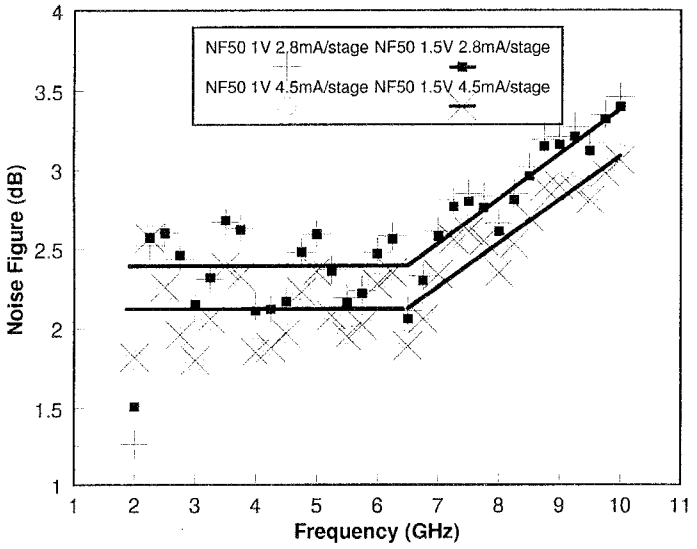

Fig. 5. 50 Ohm NF variation with supply voltage and bias current.

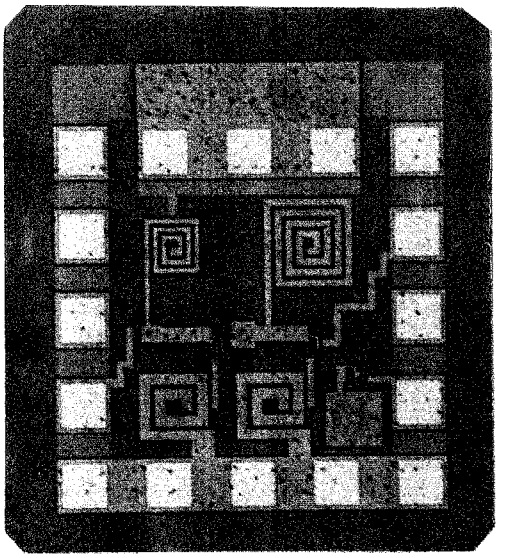

Fig. 6. Microphotograph of the 5.8GHz LNA chip. The total area is .7 x .8 mm2.

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